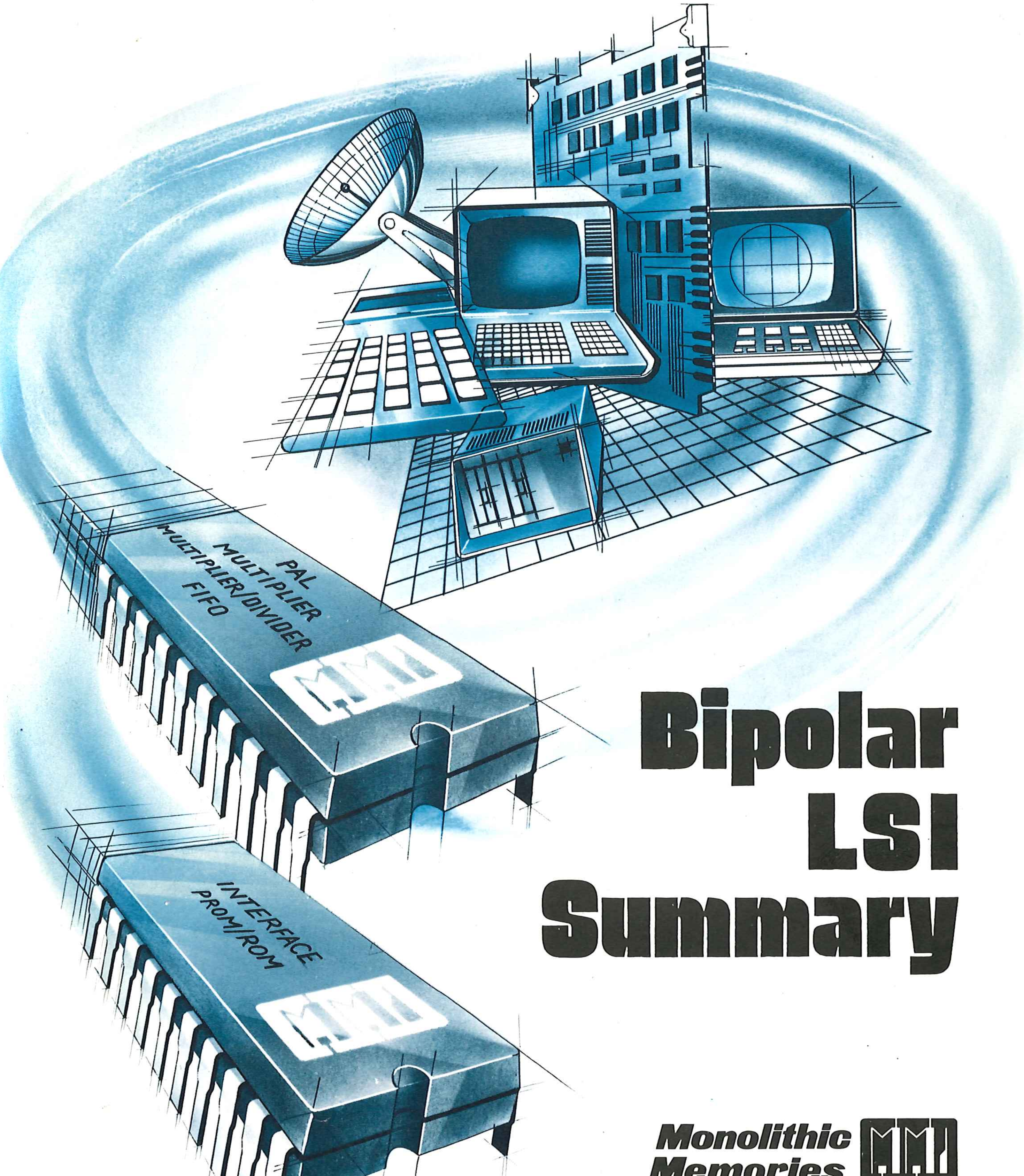
APRIL 1980



Bipolar LSI Summary

Monolithic Memories

tm2693

COMPANY PROFILE

The Company

Monolithic Memories is a company whose entire energies and resources are devoted to the development and production of bipolar LSI memory and logic devices.

Since its incorporation in 1970, Monolithic Memories has produced and delivered more bipolar memory than any other company in the world. Monolithic Memories has advanced the frontier of bipolar technology and followed it up with high-volume production.

Most of Monolithic Memories' products were industry firsts that established a clear technological and performance leadership over the competition. The world's first 1K bit PROM was introduced by Monolithic in 1971; the world's first 2K bit PROM in 1972; the first 4K bit PROM in 1975, and first 8K bit PROM in 1976.

The continuous drive for complexity led to the development of ROMs which are pin- and function-compatible with Monolithic Memories' PROMs, yet with a complexity equal to or even exceeding MOS complexities while retaining the speed and simplicity inherent in LSI bipolar process. MMI has a wide range of high-complexity ROMs such as 8K bits, 9K bits, 10K bits and 16K bits. Early in 1977 MMI introduced the world's first high-speed FIFO, which was designed to replace the slower MOS FIFO presently supplied by other manufacturers. Both products are equal in memory size, but Monolithic's FIFO is fifteen times faster than the MOS part.

Then MMI started a revolution in Logic Design. To answer the need for LSI Random Logic, a family of fuse Programmable Array Logic devices has recently been introduced. The PAL-Family utilizes advanced Schottky TTL-process and the Bipolar PROM fusible link technology to provide user programmable logic for replacing conventional SSI/MSI Gates and Flip Flop and reduced chip count and cost.

The Company's efforts are not limited to the area of memories alone. The world's first 4 bit slice was introduced by MMI, and throughout 1979 Monolithic Memories will introduce multitudes of high-complexity advanced-technology logic products.

The Company's products are presently used in a variety of applications that range from simple electronic games to highly complex microprogramming applications in a broad range of computers. At Monolithic Memories there is special emphasis placed on quality products, and the Company engages in a wide range of military programs which include both undersea and space programs.

The design, fabrication and testing of Monolithic Memories' products is done in a 100,000 square foot facility in Sunnyvale, California. The majority of the assembly is performed at a new, company-owned 30,000 square foot plant in Penang, Malaysia.

Monolithic Memories sells its products worldwide through its own sales organization, representatives and distributors. In addition to the specific sales offices in each state and in many countries in Europe, the Company has an Asian headquarters located in Tokyo, Japan.

Hi-Rel Products

All of the products at MMI were designed to operate over the entire military performance specification of ± 10% V_{CC} tolerance and $-55\ ^{o}C$ to $+125\ ^{o}C$ operating temperature ambient. Recently our 1024 bit Schottky PROM, MM5300-1/01-1 and our 2048 bit Schottky PROM, MM5305-1/06-1 was qualified to Part II of the MIL-M-38510 QPL. Other devices are in the process of QPL qualification.

Flat Packs/Chip Carriers and Die

Most of our products are available in flat packs (see individual selection guides and the package appendix for details), and our manufacturing line can accommodate your chip carrier packaging requirements as well. If your needs are for the ultimate in density, we can also supply LSI chips for your hybrid applications. These can be furnished with special 100% testing and optical inspection screens geared for hybrid packaging.

Quality System

The quality system at Monolithic Memories is based on MIL-Q-9858, "Quality Program Requirements." MIL-I-45208, "Inspection System Requirements", and MIL-M-38510, Appendix A, "Product Assurance Program". MIL-M-38510 plays a significant role in structuring MMI's quality program.

MMI's facilities in Sunnyvale were certified in June of 1977 by DESC, Defense Electronics Supply Center, to manufacture and qualify to class B and class C Schottky Bipolar PROMs, ROMs in accordance with the requirements of MIL-M-38510. This certification included a successful audit of our quality system to the stringent requirements of Appendix A of MIL-M-38510 which defines a Product Assurance Program tailored for integrated circuit manufacturers by DESC. This same quality system has also met the strict requirements of both "controlled" and "captive" line programs connected with our special Hi-Rel programs.

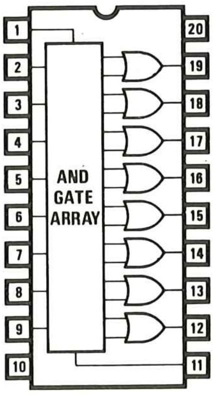
The quality accent at MMI is on process control as reflected in the use of many monitors and audits rather than gate inspections. This philosophy is consistent with building in quality and reliability rather than attempting to screen for it.

Process Control

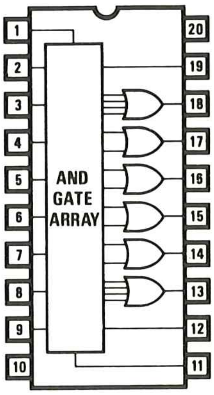
MMI's advanced low-power Schottky TTL process uses such techniques as redundant masking to reduce random defects and self-aligning masking to reduce active chip area. Although more costly than the standard SSI or MSI Schottky TTL processes, these approaches yield better quality increased reliability and lower overall cost due to higher net die per wafer. During the initial production stages of new designs and periodically thereafter, engineering characterizes the design-process compatibility by careful sample selection of lots reflecting process variable extremes.

PAL – PROGRAMMABLE ARRAY LOGIC

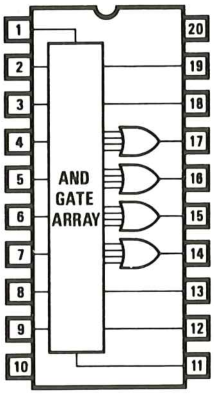
PAL10H8



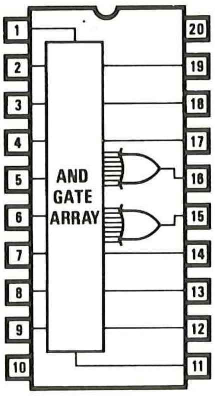
PAL12H6



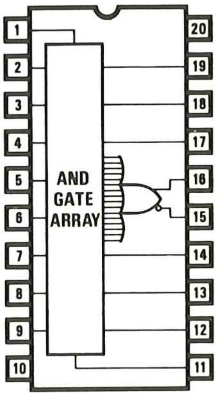
PAL14H4



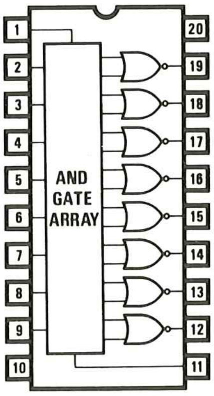
PAL16H2



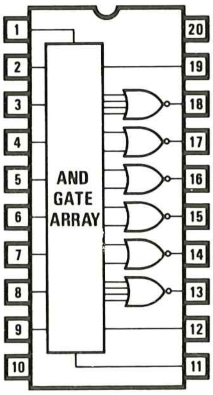
PAL16C1



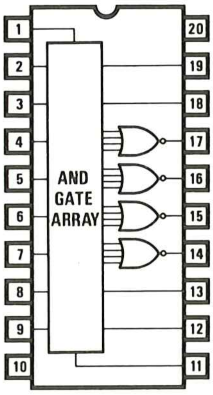
PAL10L8



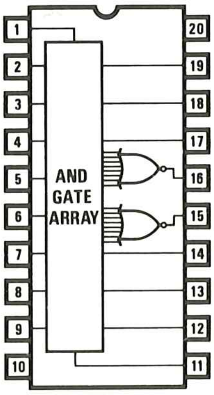
PAL12L6



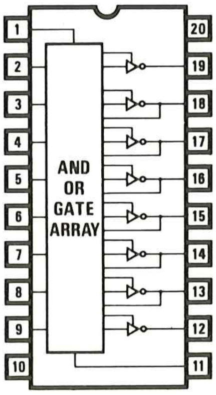
PAL14L4



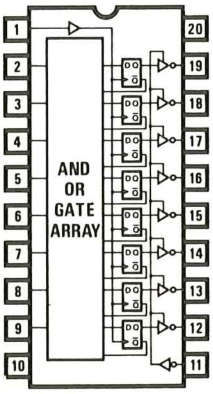
PAL16L2



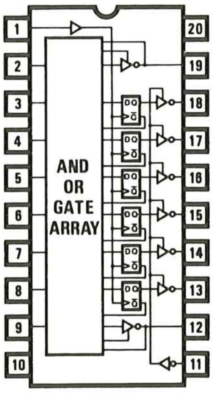
PAL16L8



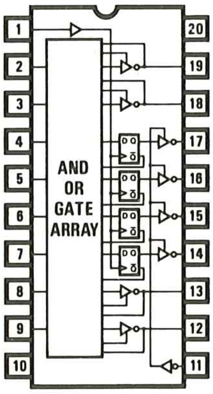
PAL16R8



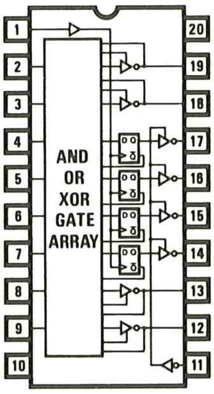
PAL16R6



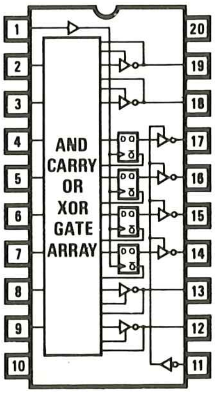
PAL16R4



PAL16X4



PAL16A4



PROGRAMMABLE LOGIC

- Programmable replacement for conventional TTL logic
- Reduces IC inventories substantially and simplifies their control
- Reduces chip count by 4 to 1
- Expediates and simplifies prototyping and board layout
- Saves space with 20 pin Skinny DIP™ packages
- High speed – tpd 25 ns typ
- Programmable on Standard PROM – and on inexpensive PAL Programmers
- Special feature eliminates possibility of copying by competitors

GATE COMPLEXITY

Type	Inputs	Progr. AND Gates	Pre-progr. Gates	OR/NOR Gates	XOR Gates	Regis-ters	TS-Buffers		Outputs
							Progr. enable	Common enable	
PAL 10H8	10	16	–	8	–	–	–	–	8
PAL 12H6	12	16	–	6	–	–	–	–	6
PAL 14H4	14	16	–	4	–	–	–	–	4
PAL 16H2	16	16	–	2	–	–	–	–	2
PAL 16C1	16	16	–	1	–	–	–	–	2
PAL 10L8	10	16	–	8	–	–	–	–	8
PAL 12L6	12	16	–	6	–	–	–	–	6
PAL 14L4	14	16	–	4	–	–	–	–	4
PAL 16L2	16	16	–	2	–	–	–	–	2
PAL 16L8	16	64	–	8	–	–	8	–	8
PAL 16R8	16	64	–	8	–	8	–	8	8
PAL 16R6	16	64	–	8	–	6	2	6	8
PAL 16R4	16	64	–	8	–	4	4	4	8
PAL 16X4	16	64	16	12	4	4	4	4	8
PAL 16A4	16	64	26	12	4	4	4	4	8

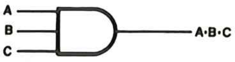
- Do not design random logic with Gates and Flip-Flops. Define your function and program it into a PAL.
- Replace many low density logic devices by few high density PAL's.
- Gain reliability and flexibility.

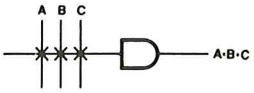
PAL's PROGRAM ON STANDARD PROM PROGRAMMERS AND CAN US

PROGRAMMABLE LOGIC

The PAL-Family utilizes an advanced Schottky TTL process and the Bipolar PROM fusible link technology to provide user programmable logic for replacing conventional SSI/MSI Gates and Flip-Flops at reduced chip count. The family enables the system engineer "to design his own chip" by blowing fusible links to configure AND/OR and FF gates to perform his desired logic function.

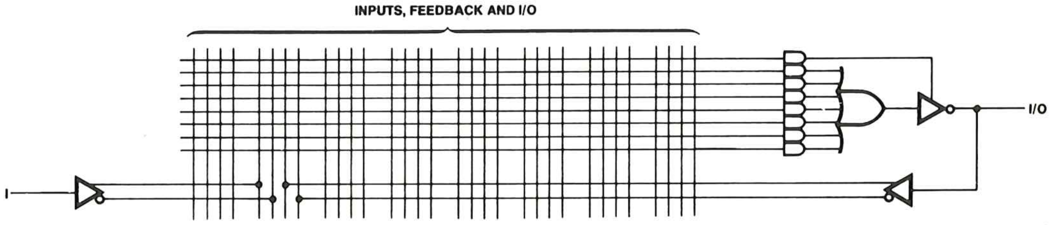
PAL-Symbology





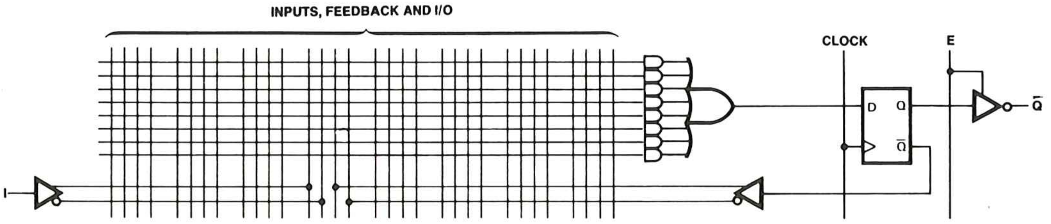
PAL's consist of few basic building blocks.
The most common is the

Programmable Input/Output Cell



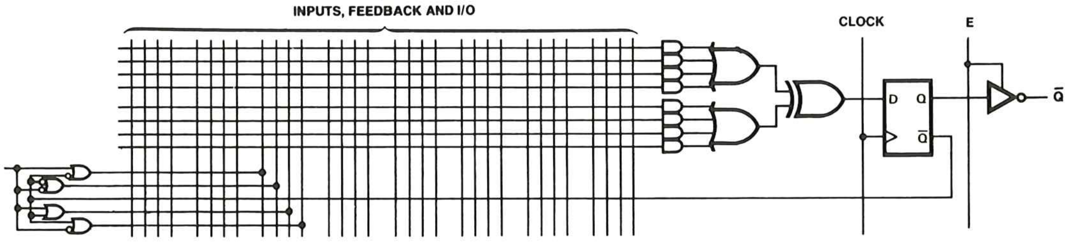
featuring 32 Input-/Feedback lines, 8 programmable AND-Gates, combined by an OR-Gate and a 24 mA three-state buffer with programmable enable.

The Registered Output with Feedback Cell



is very similar, but has a D-type, positive edge-triggered Flipflop in addition.
To perform ALU-functions and other arithmetic operations the

Arithmetic Cell



has an additional Exclusive-OR-Gate and a comparator network in the feedback lines. Additionally, one arithmetic type has up to 4 more AND-Gates, preprogrammed with carry-functions.

PAL - PROGRAMMABLE LOGIC

How to define your own PAL-Program

PAL XXXX – PAL Part No.
PAT XXXX – Customer pattern No.
Device Designation – Device Function in Circuit/Application

Pin-List

1 2 3 4 5 6 7 8 9 GND 11 12 13 14 15 16 17 18 19 V_{CC}

19 = 1*4+/2
JF (V_{CC}) 18 = 5+6+7+/8+9*11
/17: = 8*9
16 = 9*8
IF (1*2) 15 = 3+6
/14 = 3+6
IF (V_{CC}) 13 = 8*7+2

Equations
with Boolean Algebra

Description

This paragraph describes the operation of the device. Applications information like the designer's name, date or even the function table of this device may also be provided.

Operators

= Equal,. EQ.
/ Complement
* And, Product
+ Or, Sum

used by all PALs of the family

: = Replaced by following ↑, used to sign a FF-Output eg. in 16R4, R6, R8, X4, A4
IF ( ) Conditional Three State, Arithmetic, used to sign a condition in PAL 16L8, 16R6, 16R4, 16A4, 16X4.
:+: Xor, .NE. only used for the two arithmetic PALs 16X4, 16A4.

It is the responsibility of a design engineer to define the function fulfilled by PAL and document this information for future use by incoming inspection, production, final test and service departments. The above format can be used to serve this purpose.

The PAL-Assembler (PALASM) translates these equations into fuse pattern and readable data (e.g.: HEX-format) for Standard PROM-Programmer.

Fuse Pattern

```
----  ----  ----  ----  ----  ----  ----  ----
----  ----  ----  X---  ----  ----  ----  ----  5
----  ----  ----  ----  X---  ----  ----  ----  6
----  ----  ----  ----  ----  X---  ----  ----  7      One of eight
----  ----  ----  ----  ----  ----  -X--  ----  /8     programmable cells
----  ----  ----  ----  ----  ----  ----  X-X-  9*11   of PAL 16L8
XXXX  XXXX  XXXX  XXXX  XXXX  XXXX  XXXX  XXXX
XXXX  XXXX  XXXX  XXXX  XXXX  XXXX  XXXX  XXXX
```

During the Programming Cycle the PAL Device has a configuration like a 512 by 4 PROM.

2222	2222	2222	2222	2222	2222	2222	2222
2222	2222	2222	0222	2222	2222	2222	2222
2222	2222	2222	2222	0222	2222	2222	2222
2222	2222	2222	2222	2222	0222	2222	2222
2222	2222	2222	2222	2222	2222	2022	2222
2222	2222	2222	2222	2222	2222	2222	0202
0000	0000	0000	0000	0000	0000	0000	0000
0000	0000	0000	0000	0000	0000	0000	0000
0101	1111	1111	1111	1111	1111	1111	1111
1111	0111	1111	1111	1111	1111	1111	1111
1111	1111	1111	1111	0111	1111	1111	1111
0000	0000	0000	0000	0000	0000	0000	0000
0000	0000	0000	0000	0000	0000	0000	0000
0000	0000	0000	0000	0000	0000	0000	0000
0000	0000	0000	0000	0000	0000	0000	0000
0000	0000	0000	0000	0000	0000	0000	0000

Example of a translated HEX-Format for the complete PAL. Readable for PROM/PAL Programmer

These Companies Supply MMI approved PAL Personality Card Sets

Manufacturer	Personality Card Set	Socket-Adapter	Remarks
Data I/O Corporation	909-1427	715 1428-1/2/3	
Structured Design	SD 20 SD 20 A	not required H, L, C, R, X decoding by switch	— PALASM integrated
Pro-Log Corporation	PM 9068		
STAG-Systems	PM 202	AM 10H8, AM 12H6, AM 14H4, AM 16H2, AM 10L8, AM 12L6, AM 14L4, AM 16L2, AM 16C1	
Cybernetic Programming System Inc.	CYMPL-1		PALASM integrated

PROM
STANDARD FAMILY

Organization	Package	T_{AA} max. (ns)	Open Collector	Three state
256×4	16	55	6300-1	6301-1
512×4	16	60	6305-1	6306-1
1024×4	18	60	6350-1	6351-1
1024×4	18	60	6352-1	6353-1
32×8	16	50	6330-1	6331-1
256×8	20	70	6308-1	6309-1
256×8	24	70	6335-1	6336-1
512×8	20	70	6348-1	6349-1
512×8	24	70	6340-1	6341-1
1024×8	24	90	6380-1	6381-1

- Commercial and military temperature range
- JAN/QPL part available
- Compatible up grade pin configurations
- 4-bit-wide and 8-bit-wide for byte orientated applications
- single +5 V Supply Voltage
- High reliable Schottky Process with NiCr Fuses
- Low fan-in (MOS-compatible) 250 µA
- Pin compatible ROMs available

High Performance PROMs – preliminary information

Organization	Package	High speed		Low power		Registered		Power switched	
		OC	TS	OC	TS	Async.	Sync.	OC	TS
256×4	16	63S140	63S141	63LS140	63LS141	–	–	63PS140	63PS141
512×4	16	63S240	63S241	63LS240	63LS241	–	–	63PS240	63PS241
1024×4	18	63S440	63S441	63LS440	63LS441	63RA441	63RS441	63PS440	63PS441
2048×4	18	63S840	63S841	63LS840	63LS841	–	–	63PS840	63PS841
2048×4	20	–	–	–	–	63RA841	63RS841	–	–
4096×4	20	63S1640	63S1641	63LS1640	63LS1641	63RA1641	63RS1641	63PS1640	63PS1641
32×8	16	63S080	63S081	63LS080	63LS081	–	–	–	–
256×8	20	63S280	63S281	63LS280	63LS281	–	–	63PS280	63PS281
256×8	24S	–	–	–	–	63RA283	–	–	–
512×8	20	63S480	63S481	63LS480	63LS481	–	–	63PS480	63PS481
512×8	24	63S482	63S483	63LS482	63LS483	–	–	63PS482	63PS483
512×8	24S	–	–	–	–	63RA483	–	–	–
1024×8	24	63S880	63S881	63LS880	63LS881		–	63PS880	63PS881
1024×8	24S	–	–	–	–	63RA883	–	–	–
2048×8	24	63S1680	63S1681	63LS1680	63LS1681	–	–	63PS1680	63PS1681
2048×8	24S	–	–	–	–	63RA1683	–	–	–

- Largest PROM-Family planned
- Generic Family by DC-Parameters and Programming Specs.

PROM – Speed Selection Guide / max. address access time (TAA) in nanoseconds

Organization	Standard Family	High Performance Family			
		High speed	Standard	Low power	Switched
256×4	55	35	45	55	45
512×4	60	35	45	55	45
1024×4	60	40	50	65	50
2048×4	–	50	60	75	60
4096×4	–	–	70	85	70
32×8	50	–	25	35	–
256×8	70	–	45	60	45
512×8	70	–	45	60	45
1024×8	90	–	50	65	50
2048×8	–	–	70	85	70

- All families are pincompatible and interchangeable

OCTAL INTERFACE PRODUCTS

Description

The Microprocessor Interface Series 54/74 Schottky and Low Power Schottky Octal Buffer, Transceiver, Latch and Register Familiy is selected specific for use in microprocessor design applications. The Schmitt-Trigger operation makes the LS buffer ideal for bus receivers in a noisy environment. The Schmitt-Trigger operation on the S buffers acts as a safeguard against feedback oscillation and prevents slow transition through the threshold region, insuring fast transition and reducing the spikes.

Octal Latches, Octal Registers with Three-State Outputs

Part Number	Package	Temp.	I_{OL}	Polarity	Type	Power
SN74LS373 SN54LS373	N, J J	com mil	24 mA 12 mA	Non-invert	Latch	LS
67LS380 57LS380	N, J J	com mil	24 mA 12 mA	Invert		
SN74LS374 SN54LS374	N, J J	com mil	24 mA 12 mA	Non-invert	Register	
67LS376 57LS376	N, J J	com mil	24 mA 12 mA	Invert		
SN74S373 SN54S373	N, J J	com mil	20 mA	Non-invert	Latch	S
67S373 57S373	N, J J	com mil	32 mA			
67S380 57S380	N, J J	com mil	20 mA	Invert		
67S382 57S382	N, J J	com mil	32 mA			
SN74S374 SN54S374	N, J J	com mil	20 mA	Non-invert	Register	
67S374 57S374	N, J J	com mil	32 mA			
67S376 57S376	N, J J	com mil	20 mA	Invert		
67S378 57S378	N, J J	com mil	32 mA			

Octal Buffers

Part Number		Package	Temp.	Enable	Polarity	Threshold
S	LS					
SN74S240 SN54S240	SN74LS240 SN54LS240	N, J J	com mil	LOW	Invert	Hysteresis
67S306 57S306	67LS306 57LS306	N, J J	com mil	LOW-HIGH		
SN74S244 SN54S244	SN74LS244 SN54LS244	N, J J	com mil	LOW	Non-invert	
SN74S241 SN54S241	SN74LS241 SN54LS241	N, J J	com mil	LOW-HIGH		
67S300 57S300	67LS300 57LS300	N, J N	com mil	LOW	Invert	Schmitt trigger
67S307 57S307	67LS307 57LS307	N, J N	com mil	LOW-HIGH		
67S304 57S304	67LS304 57LS304	N, J N	com mil	LOW	Non-invert	
67S301 57S301	67LS301 57LS301	N, J N	com mil	LOW-HIGH		

Octal Transceivers

Part Number	Type	Temp.	Polarity	Threshold
SN74LS245 SN54LS245	N, J J	com mil	Non-invert	Hysteresis
SN74LS645 SN54LS645	N, J J	com mil	Non-invert	Hysteresis

Features

- 20-Pin SKINNY DIP™ saves space
- Three-state outputs drives bus lines
- Ideal for microprogram instruction register
- Low current PNP inputs reduce loading
- 8-bits match byte boundaries
- Ideal for microprocessor interface
- Inverting and non-inverting outputs
- Schmitt-Trigger guarantees high noise margin
- Synchronous or asynchronous clear
- I/O part enables output data back to input bus
- Ideal for microprocessor I/O parts
- MIL and HIREL specs. available
- Comparable R_{th} N Package results to J Package

MMI PART NUMBER CODES

Standard Products

6241-1J

Temperature Range
- 5 = Military
- 6 = Commercial

Product Type
- 0 = Character Generator
- 2 = Read Only Memory
- 3 = Programmable Read Only Memory
- 7 = LSI Computer Logic Product

Process
- -1 = Schottky TTL Process (on PROM s and ROMs)
- -2 = Improved version of -1 part

Package
- J = CERDIP
- D = Ceramic (side brazed)
- F = Flat pack

PAL Series 20

PAL14L4CJ

Programmable Array Logic Family

Number of Array Inputs

Output Type
- H = Active HIGH
- L = Active LOW
- C = Complementary
- R = Registered
- X = Exclusive-OR Registered
- A = Arithmetic Registered

Number of Outputs

Temperature Range
- C = 0 °C to +75 °C
- M = –55 °C to +125 °C

Package
- J = Ceramic DIP

High Performance Schottky PROMs

5 3 S 4 8 0 A J = Military High Speed 4096 PROM organized 512 x 8 with open collector outputs

Temperature Performance Range
- 5 = Military
- 6 = Commercial

Memory Type
- 3 = PROM (Fuse Programmable)
- 2 = ROM (Mask Programmable)

Generic Family Designator
- S = Schottky
- LS = Low Power Schottky
- PS = Power Switched Schottky
- RA = Registered Asynchronous, Schottky
- RS = Registered Synchronous, Schottky

Size of Memory
- 0 = 256 Bit
- 1 = 1024 Bit
- 2 = 2048 Bit
- 4 = 4096 Bit
- 8 = 8192 Bit
- 16 = 16384 Bit

Number of Outputs
- 4 = 4 Outputs
- 8 = 8 Outputs

Output/Pinout Designator
- 0 = Open Collector } 1st pkg. (i.e., 20 pin)
- 1 = Tri-State
- 2 = Open Collector } 2nd pkg. (i.e., 24 pin)
- 3 = Tri-State

etc., etc., etc.

Performance

Absence of letter indicates standard performance.
- A = enhanced (i.e., speed)

Package
- J = Cerdip
- D = Side brazed
- N = Plastic
- F = Flatpack

TECHNICAL LITERATURE

Data Books

Bipolar LSI Data Book
PAL Handbook

Data Sheets

Standard PROM Family
PROM Selection Guide and Cross Reference
PAL Data Sheet
FIFO Data Sheet
67558 Multiplier 8x8
67516 Multiplier/Divider 16x16
Interface Data Sheet

Application Notes

PROM Standard Family
A new generation of bipolar PROMs
Power Switch ROMs and PROMs
PAL Assembler
FIFO-Application
Multiplier-Application

Reliability-Reports

-1 Series Reliability Report
Plastic Package
24pin Cerdip Package
Reliability Assessment of Bipolar PROMs

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